A LOW COST PACKAGING/TESTING PROCEDURE FOR MANUFACTURING GaAs MMIC

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ABSTRACT

The development of a low cost, high throughput testing/packaging procedure for GaAs MMIC is described. Automated on-wafer RF and DC testing is essential for volume production of MMIC chips. However, most MMIC circuits cannot be tested at wafer level due to lack of proper RF test environment. The proposed frame tape chip carrier approach takes full advantage of the RF probe system. This technique reduces the high cost of RF package measurements and reliability testing. The measurement and packaging is demonstrated on several MMIC chips. It can easily be automated for high volume production.

INTRODUCTION

GaAs MMIC have promised high potential for reducing microwave system cost. Since the cost of microwave packaging and testing is a significant portion of MMIC production cost, it is clear that low cost packaging and testing procedures must be developed. Furthermore, to accomplish the overall objective of manufacturing large quantities of MMICs for space and military application yields, performance and reliability must be considered in the packaging methodology.

The development of the proposed packaging philosophy is based on the following assessment: 1) Automated on-wafer RF probing is available now, however, most circuits cannot be tested at wafer level before thinning, due to lack of RF ground and lack of physical DC ground connections (via holes) to devices. 2) Most MMIC design rules require thinning the wafer to a thickness of 4 to 5 mils. This increases the risk of wafer breakage. Therefore, wafer handling must be minimized at the tail-end processing step. 3) Yield loss due to tail-end processing and die attachment makes it preferable to do the final chip acceptance test at the end of tail-end processing and die attachment. 4) The traditional way of RF testing of MMIC chips (packaging chips into test fixtures) is slow and labor intensive. The proposed packaging technique utilizes batch on-chip RF probing and also reduces the burn-in and life test cost.

TESTING/PACKAGING METHODOLOGY

This packaging technique is based on a two level (bare chip on carrier and module level) packaging concept. The MMIC chips are mounted on a multiple chip carrier. (Frame tape, Figure 1). Frame tape is a thin strip of special gold-plated alloyed material etched to a configuration that facilitates mounting a number of GaAs MMIC chips. The chip carriers are etched to the proper MMIC size and remain attached to the frame tape until the final on-chip RF probe acceptance test is performed. The frame provides support for the chip carrier and the chip carrier supports the MMIC die. Another advantage of bare chip on frame tape carrier is in multichip module or hybrid/monolithic assemblies. Some circuit types are never packaged by themselves, but are immediately assembled into larger hybrid modules or assemblies. These circuits present special problems from verifying RF performance to costly rework of the multichip module or assembly. This carrier concept allows the chips to be mounted for RF measurements as well as burn-in, life and other reliability tests. The chips can be accessed by using CASCADE RF [1,2] probes, and after the tests, the chip carrier is separated from the frame tape and dropped into the module or assembly. This technique can be used for power devices since the chip carrier will provide adequate heat sinking of the chip.

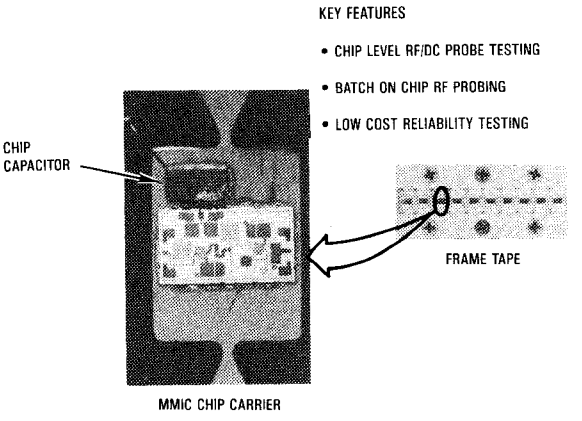

Figure 1. Frame Tape MMIC Chip Carrier for Multichip RF Testing and Packaging

The overall GaAs MMIC testing and first level packaging flow plan is depicted in Figure 2. Wafer level testing is limited to DC functional screening of circuits and RF testing of FET. If the FET RF yield is poor or out of specification, the wafer is rejected and will not go through the expensive tail-end process (thinning, dicing and assembly). For a good wafer only DC functional chips are selected. The chips are mounted on the frame chip carrier. At this point the RF functionality is checked with the RF probe card. The nonworking chips are either reworked or rejected. The DC burn-in and

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life test is performed next. The chips are checked for RF functionality, detached from the fame tape and mounted into package or multichip module.

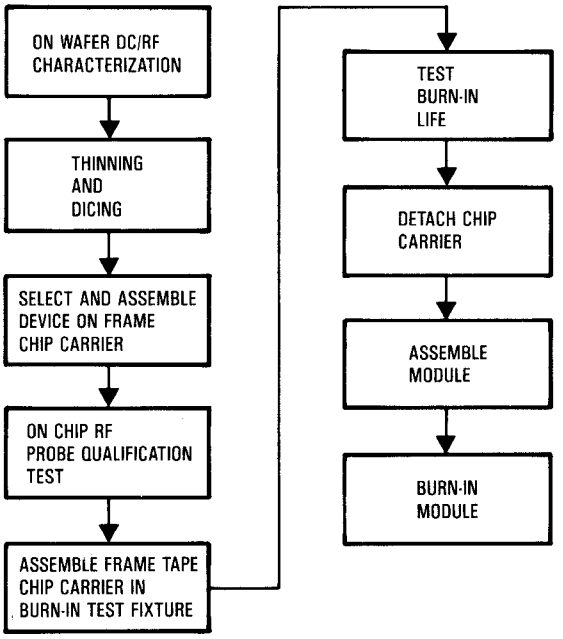

Figure 2. Testing and Packaging Flow Plan

Figure 3 demonstrates testing and packaging procedure.

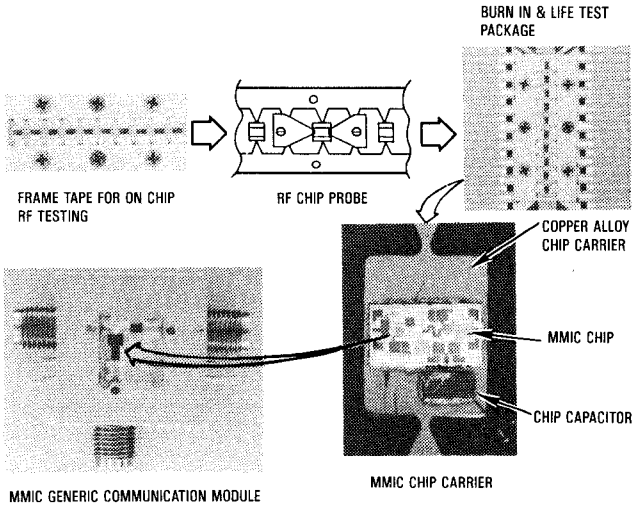

Figure 3. New GaAs MMIC Packaging Concept RF, DC/Burn In/Life Test

The burn-in and life test is done in batches of several hundred by mounting the tape into the burn-in fixture block. Such a fixture is shown in Figure 4.

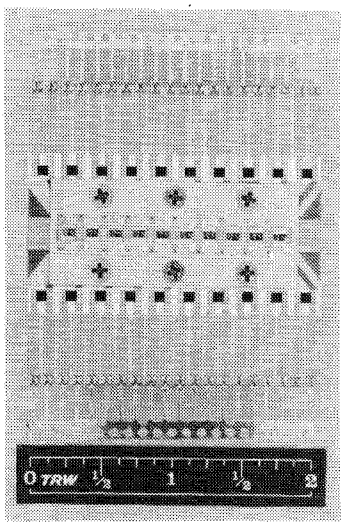

Figure 4. Life and Burn-In Test Fixture

The DC connection to the MMIC chip is done via a chip capacitor. This will eliminate any rework on the DC connection pads of the MMIC chip. The MMIC chip RF parts are formatted to facilitate on-chip RF probing. Figure 5 shows examples of three MMIC chips designed for on-chip RF probing. The chips are 1-4 GHz IF amplifier, 6-10 GHz low noise amplifier and a 1-18 GHz distributed amplifier. Two grounds are provided on each part for coplanar waveguide [3] to microstrip line transition.

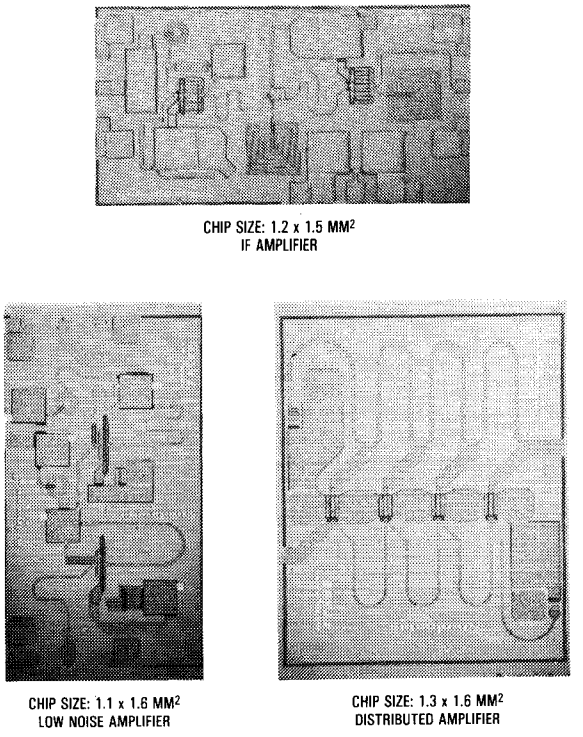

Figure 5. Three GaAs MMIC Chips, Layout Formatted for On-Chip RF Probing

Figure 6 shows test results of MMIC chips measured on chip with RF probe.

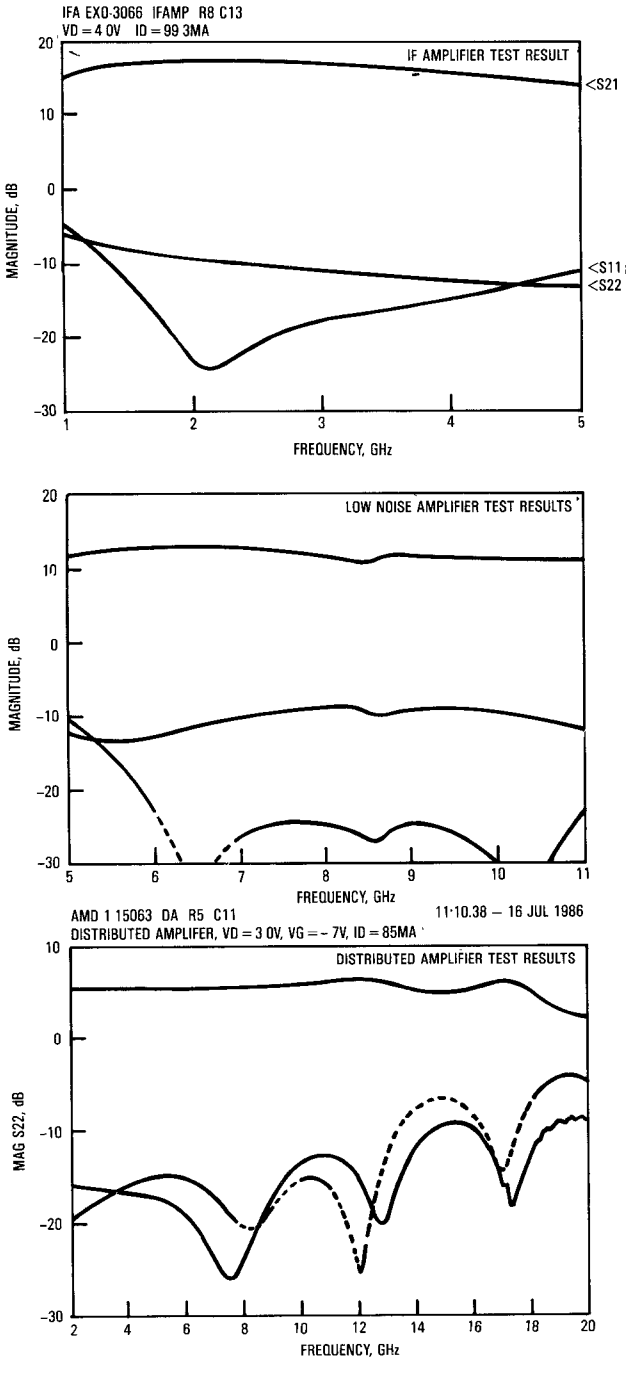

Figure 6 Test Results of MMIC Chips Measured on Chip With RF Probe

For existing application the frame tape is cut to support 10 MMIC chips. The gain of 10, IF amplifier-measured on frame tape, after 168 hours burn-in is shown in Figure 7. All 10 chips DC-tested good before chip assembly and wire bonding. Nine chips RF tested good after assembly and wire bond. The burn-in and reliability results will be presented elsewhere. With bare chip on frame tape carrier technique, die attachment and the RF testing can be easily automated.

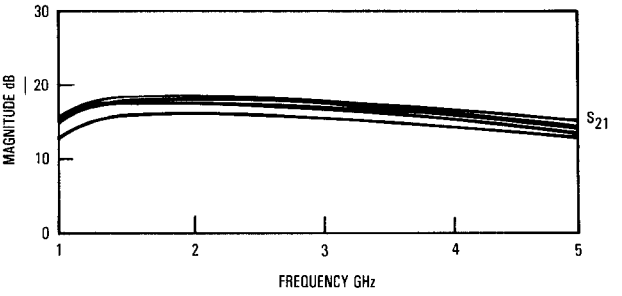

Figure 7 Gain of 10, IF Amplifier-Measured, on Frame Tape After 168 Hrs Burn-in

CONCLUSIONS

The development of a low cost testing/packaging procedure for GaAs MMIC has been described. Automated on-wafer RF and DC testing is essential for volume production of MMIC chips. The RF testing of MMIC chips at the wafer level currently is viewed as yielding little useful information due to the inability to provide a proper RF test environment.

Due to lack of RF and DC grounding, most MMIC circuits cannot be tested at wafer level before thinning out back side process. The proposed frame tape chip carrier approach takes full advantage of RF probe system. With this technique the high cost of RF packaged measurement and reliability testing is reduced. It can easily be automated.

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